WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate,

a plurality of memory cells arranged in the form of a matrix on said semiconductor substrate, each of said memory cells including transistors having floating gate electrodes and control gate electrodes;

element isolation insulating films for isolating said memory cells; and

source lines formed in a self-alignment manner with respect to said control gate electrodes;

wherein the surface of said semiconductor substrate has such a periodical unevenness along said source lines that the portions of said memory cells form projection portions and the portions where said element isolation insulating films have removed form recess portions;

each of said source lines has a diffusion layer in which an impurity is distributed along the surface of said semiconductor substrate and a buried diffusion layer in which an impurity is distributed at a position deeper than said diffusion layer;

and said buried diffusion layer connects a plurality of portions of said diffusion layers under the bottom surface of said recess portion to each other.

2. The nonvolatile semiconductor memory device according to claim 1, wherein said diffusion layer and said buried diffusion layer is connected each other at said projection portion.

3. The nonvolatile semiconductor memory device according to claim 1, wherein said source line is at a ground level or in an floating state in any of write, erase, and read operations.

4. The nonvolatile semiconductor memory device according to claim 2, wherein said source line is at a ground level or in an floating state in any of write, erase, and read operations.